REMARKS

Claims 1-7, 9-20, and 22 are now pending in the application. Claims 8 and 21 are cancelled without disclaimer or prejudice to the subject matter contained therein. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

Applicant would like to thank the Examiner for the courtesy extended during the personal interview conducted on January 23, 2007. During the interview, Applicant's representative and the Examiner discussed independent claim 11 in view of Anderson.

REJECTION UNDER 35 U.S.C. § 102

Claims 1, 3, 5 and 6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kolinski et al. (U.S. Pat. No. 6,092,207). This rejection is respectfully traversed.

With respect to claim 1, Kolinski fails to show, teach, or suggest providing power to an integrated circuit (IC) during an active mode, moving an integrated circuit state of the IC into on-die storage of the IC, and externally disabling power to on-die combinational circuitry during a low power mode by disrupting power supplied from an external power supply regulator to the IC.

In particular, Kolinski appears to be absent of any teaching or suggestion of moving an integrated circuit state into on-die storage of the IC, and instead discloses storing a state of the computer in external RAM.

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. *Scripps Clinic & Res. Found. V. Genentech, Inc.*, 18 USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be inherent or expressly disclosed and must be arranged as in the claim. *Constant v. Advanced Micro-Devices, Inc.*, 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, Kolinski fails to disclose the limitation of moving the IC state into on-die storage of the IC.

In contrast, **Kolinski appears to disclose moving the IC state to off die storage, not on-die storage of the IC**. The Examiner cites Column 4, Lines 23-43 and Lines 55-67, and Column 5, Lines 46-57. Applicant respectfully notes that the cited portions of Kolinski disclose transferring the state of the computer to an external RAM array (i.e. off-die storage). For example, "[w]hen the computer is placed in a suspend-to-RAM mode, the state of the computer is stored in RAM (DRAM memory array 265)." (See Column 4, Lines 28-29). As shown in FIGS. 2 and 3, the DRAM memory array 265 is not located on-die with respect to the host processor 285. In particular, FIG. 3 illustrates that the host processor 285 is located on a motherboard and the DRAM memory array 265 is not located on the motherboard.

Applicant respectfully submits that Kolinski fails to show, teach, or suggest moving an IC state of the IC to on-die storage of the IC. Claim 1, as well as its dependent claims, should be allowable for at least the above reasons.

Claims 7, 8 and 10 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Stapleton et al. (U.S. Pat. No. 6,574,577 B2). This rejection is respectfully traversed.

With respect to claim 7, Stapleton fails to show, teach, or suggest forcing a high impedance state on an output of a power supply regulator that is coupled to a power pin of an integrated circuit, wherein forcing the high impedance state includes de-asserting a drive pin coupled to a gate of a MOS power transistor to force the high impedance state on the output of the power supply regulator. In particular, Stapleton appears to be absent of any teaching or suggestion of **de-asserting a drive pin coupled to a gate of a MOS power transistor to force the high impedance state**.

The Examiner alleges that Stapleton discloses this structure at Column 2, Lines 38-50. The cited portion of Stapleton states:

> For example, the power good circuit 16 asserts (drives high, for example) the PWR_GOOD signal to indicate a valid V_{TT} voltage and thus, to cause the voltage regulator 14 to provide the V_{CCP} voltage to the supply voltage plane 15. The power good circuit 16 de-asserts (drives low, for example) the PWR_GOOD signal to indicate an invalid V_{TT} voltage and cause the voltage regulator 14 to tri-state its output terminal and not provide the V_{CCP} voltage to the supply voltage plane 15. As described below, the power good circuit 16 regulates the timing of its assertion of the PWR_GOOD signal to ensure that the processor's indication of its VID number is valid when the voltage regulator 14 generates the V_{CCP} voltage.

Applicant respectfully notes that the above cited portion appears to be absent of any teaching or suggestion of a MOS power transistor, and is particularly absent of any teaching or suggestion of de-asserting a drive pin coupled to a gate of a MOS power transistor.

Applicant respectfully submits that claim 7, as well as its dependent claims, should be allowable for at least the above reasons.

Claims 11 and 17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Anderson et al. (U.S. Pat. No. 5,999,386). This rejection is respectfully traversed.

With respect to claim 11, Anderson fails to show, teach, or suggest a first terminal of an integrated circuit (IC) coupled to receive power for on-die combinational circuitry when the integrated circuit is in an active mode and to not receive power when the integrated circuit is in a low power mode, and a second terminal to receive power supplied to circuitry for low power logical state retention of the IC when the integrated circuit is in the low power mode, wherein the second terminal provides power to low-leakage memory that stores the logical state.

In an exemplary embodiment shown in FIG. 1 of the present application, a second terminal 150 receives power supplied to circuitry **for low power logical state retention of the IC** during the low power mode. The Examiner relies on pin 30 to disclose this second terminal. Applicant respectfully notes that the IC of Anderson receives a constant power supply signal that "remains at a high logic level when the IC is power up and operating in either a normal operating mode or a sleep mode." (See Column 6, Lines 44-47). More specifically, the pin 30 provides the constant power supply signal to an electrostatic discharge (ESD) protection circuit 52 and an input and drive circuit portion 48. In other words, the pin 30 does not appear to provide power for low power logical state retention of the IC, and instead provides power to the ESD protection circuit 52 and the input and drive circuit portion 48.

Further, claim 11 recites that the second terminal provides power to low-leakage memory that stores the logical state of the IC. Neither the cited portion, nor any other portion of Anderson appears to disclose that the alleged pin 30 **provides power to low-leakage memory for low power logical state retention of the IC**.

Applicant respectfully submits that claim 11, as well as its dependent claims, should be allowable for at least the above reasons.

Claims 18 and 22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Lu et al. (U.S. Pat. No. 6,064,223). This rejection is respectfully traversed.

With respect to claim 18, Lu fails to show, teach, or suggest a multiplexer that selectively connects an external power signal supplied at a pin of the integrated circuit, an internal power signal of the integrated circuit, and a power signal supplied to the external control transistor to the power supply.

As shown in an exemplary embodiment in FIG. 5 of the present application, a multiplexer 520 selectively outputs a signal to a power supply regulator 110. The multiplexer 520 receives inputs from various points along a path between the power supply regulator and an integrated circuit. For example, a first input is connected to the power signal at an input of clamp transistors 510. A second input is connected to the power signal at the external pin 130. A third input is connected to an internal portion of the integrated circuit. In other words, the multiplexer 520 selectively connects an external power signal supplied at a pin of the integrated circuit, an internal power signal of the integrated circuit, and a power signal supplied to the external control transistor to the power supply.

Applicant respectfully submits that Lu fails to disclose this structure. For example, the Examiner relies on Column 2, Line 63 though Column 3, Lines 4 to disclose a multiplexer:

> For example, gates, including but not limited to, NOR gates or NAND gates could be used to logically determine when standby mode is to be entered as well as to switch between the voltages appropriate for driving the gate terminals of the FETs used as switchable pathways. **Similarly,**

> **FETs configured in a multiplexer arrangement, sometimes referred to as a transmission gate, can be used to couple the gate terminal of a FET used as switchable pathway to various power supply nodes.** (Emphasis added).

Applicant respectfully notes that the cited portion only generally discloses a multiplexer and fails to disclose the specific structure of the multiplexer as claim 18 recites. In particular, the cited portion discloses a multiplexer that couples a gate terminal of a transistor to various power supply nodes, and fails to disclose selectively connecting a power supply to a power signal path at an external control transistor, an external power signal, and an internal power signal as claim 18 recites.

Applicant respectfully submits that claim 18, as well as its dependent claims, should be allowable for at least the above reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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